What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a main surface that includes a power MOSFET formation region having a first trench for forming a power MOSFET thereon and a peripheral device formation region having a second trench for forming a peripheral device thereon, the semiconductor substrate surrounding the first trench being for working as a drain of the power MOSFET; and

a well layer of a second conductivity type disposed in the second trench of the peripheral device formation region.

2. The semiconductor device according to claim 1, wherein:

the power MOSFET comprises;

a drift region of the first conductivity type, disposed in the first trench and having an impurity concentration lower than that of the semiconductor substrate;

a base region of the second conductivity type, disposed in the drift region and extending from the main surface in a perpendicular direction with respect to to the main surface;

a source region of the first conductivity type, disposed in the base region and extending from the main surface in the perpendicular direction;

a gate insulating film disposed on a surface of a

third trench that extends from the main surface in the perpendicular direction and penetrates the source region and the base region; and

a gate electrode disposed on the gate insulating film and filling the third trench; and

the peripheral device comprises;

a semiconductor layer of the first conductivity type having an impurity concentration lower than that of the semiconductor substrate, and disposed in the second trench; and

the well layer disposed in the semiconductor layer.

3. The semiconductor device according to claim 2, wherein the second trench has a depth that is equal to or less than a thickness of the drift region.

4. The semiconductor device according to claim 2, wherein the second trench has a width that is twice or less than twice as large as a thickness of the drift region.

5. The semiconductor device according to claim 2, wherein the second trench has a depth that is equal to or less than a sum of a thickness of the drift region and a thickness of the base region.

6. The semiconductor device according to claim 2, wherein the second trench has a width that is equal to or

less than twice as large as a sum of a thickness of the drift region and a thickness of the base region.

7. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type disposed on a surface of the semiconductor substrate and having a main surface at an opposite side of the semiconductor substrate;

a power MOSFET formed in a first trench that extends from the main surface of the semiconductor layer, penetrates the semiconductor layer, and reaches the semiconductor substrate, the power MOSFET comprising:

a drift region of the first conductivity type disposed in the first trench and having an impurity concentration lower than that of the semiconductor substrate;

a base region of the second conductivity type formed in the drift region and extending from the main surface in a perpendicular direction with respect to the main surface;

a source region of the first conductivity type formed in the base region and extending from the main surface in the perpendicular direction;

a gate insulating film disposed on a surface of a second trench that extends from the main surface in the perpendicular direction and penetrates the source region and the base region; and

a gate electrode disposed on the gate insulating film and filling the second trench; and

a peripheral device provided in the semiconductor layer at a region different from a region where the power MOSFET is provided.

8. The semiconductor device according to claim 7, further comprising an insulating film disposed between the semiconductor substrate and the semiconductor layer.

9. A method for manufacturing a semiconductor device, comprising:

preparing a semiconductor substrate of a first conductivity type having a main surface that has a power MOSFET formation region for forming a power MOSFET and a peripheral device formation region for forming a peripheral device;

forming a first trench at the power MOSFET formation region on the semiconductor substrate;

forming a second trench at the peripheral device formation region on the semiconductor substrate;

forming a first semiconductor film of the first conductivity type on the main surface and on sidewalls of the first and second trenches, the first semiconductor film having an impurity concentration lower than that of the semiconductor substrate;

forming a second semiconductor film of a second

conductivity type on the first semiconductor film;

forming a third semiconductor film of the first conductivity type on the second semiconductor film, the third semiconductor film having an impurity concentration higher than that of the first semiconductor film; and

flattening a surface of the first to third semiconductor films forming a three-layered structure, wherein:

the first trench is sized so that all of the first to third semiconductor films are disposed in the first trench to form the power MOSFET in which the first semiconductor film constitutes a drift region, the second semiconductor film constitutes a base region, and the third semiconductor film constitutes a source region; and

the second trench is sized so that at least the first semiconductor film is disposed in the second trench.

10. The method according to claim 9, wherein the second trench is formed at a depth that is equal to or less than a thickness of the first semiconductor film.

11. The method according to claim 9, wherein:

the first trench and the second trench are formed simultaneously;

the second trench is formed with a width that is twice or less than twice as large as a thickness of the first semiconductor film.

12. The method according to claim 9, wherein:

the first trench and the second trench are formed simultaneously;

the second trench is formed at a depth that is equal to or less than a sum of a thickness of the first semiconductor film and a thickness of the second semiconductor film.

13. The method according to claim 9, wherein:

the first trench and the second trench are formed simultaneously;

the second trench is formed with a width that is twice or less than twice as large as a sum of a thickness of the first semiconductor film and a thickness of the second semiconductor film.

14. The method according to claim 9, wherein the first to third semiconductor films are epitaxially grown.

15. The method according to claim 9, wherein:

the first semiconductor film is formed by an epitaxial growth;

the second semiconductor film is formed by inverting the conductivity type of a surface portion of the first semiconductor film from the first conductivity type into the second conductivity type; and

the third semiconductor film is formed on the second semiconductor film by the epitaxial growth.

16. A method for manufacturing a semiconductor device, comprising:

preparing a semiconductor substrate of a first conductivity type having thereon a semiconductor layer of a second conductivity type;

forming a trench from a surface of the semiconductor layer in a perpendicular direction with respect to the surface so that the trench reaches the semiconductor substrate;

forming a first semiconductor film of the first conductivity type on the surface of the semiconductor layer and on a sidewall of the trench, the first semiconductor film having an impurity concentration lower than that of the semiconductor substrate;

forming a second semiconductor film of the second conductivity type on the first semiconductor film;

forming a third semiconductor film of the first conductivity type on the second semiconductor film, the third semiconductor film having an impurity concentration higher than that of the first semiconductor film; and

flattening a surface of the first to third semiconductor films forming a three-layered structure, wherein:

the trench is sized so that all of the first to third

semiconductor films are disposed in the trench to form a power MOSFET in which the first semiconductor film constitutes a drift region, the second semiconductor film constitutes a base region, and the third semiconductor film constitutes a source region ; and

a peripheral device is formed in the semiconductor layer except a region where the power MOSFET is provided.

17. The method according to claim 16, wherein the semiconductor layer is disposed on the semiconductor substrate with an insulating layer interposed therebetween.

18. The method according to claim 16, further comprising, forming a fourth semiconductor film on the sidewall of the trench before the first semiconductor film is formed, the forth semiconductor film having an impurity concentration higher than that of the first semiconductor film.

19. The method according to claim 16, wherein the first to third semiconductor films are epitaxially grown.

20. The method according to claim 16, wherein:

the first semiconductor film is formed by an epitaxial growth;

the second semiconductor film is formed by inverting the conductivity type of a surface portion of the first

semiconductor film from the first conductivity type into the second conductivity type; and

the third semiconductor film is formed on the second semiconductor film by the epitaxial growth.

21. A semiconductor device comprising:

a first conductivity type semiconductor substrate;

a power MOSFET formed in the semiconductor substrate at a power MOSFET formation region, the power MOSFET including a drain that is composed of the semiconductor substrate;

a peripheral device formed in the semiconductor substrate at a peripheral device formation region; and

a semiconductor region surrounding the peripheral device to separate the peripheral device from the semiconductor substrate, and having an impurity concentration lower than that of the semiconductor substrate.

22. The semiconductor device according to claim 21, wherein the semiconductor region is provided in a trench provided in the semiconductor substrate at the peripheral device formation region.

23. The semiconductor device according to claim 22, wherein the semiconductor region is composed of a first conductivity type semiconductor region having an impurity concentration lower than that of the semiconductor substrate

and disposed on an inner wall of the trench, and a second conductivity type semiconductor well region provided in a surface portion of the first conductivity type semiconductor region.

24. The semiconductor device according to claim 21, wherein:

the power MOSFET is provided in a first trench of the semiconductor substrate;

the semiconductor region in which the peripheral device is provided is provided in a second trench of the semiconductor substrate, the second trench being different from the first trench in size.

25. The semiconductor device according to claim 24, wherein at least one of a width and a depth of the second trench is smaller than that of the first trench.

26. The semiconductor device according to claim 21, wherein;

the semiconductor region is disposed on a surface of the semiconductor substrate;

the power MOSFET is provided in a trench extending from a surface of the semiconductor region and penetrating the semiconductor region to reach the semiconductor substrate that works as the drain of the power MOSFET; and

the peripheral device is formed in the semiconductor

region apart from the trench.

27. The semiconductor device according to claim 26, wherein the semiconductor region has a second conductivity type.

28. The semiconductor device according to claim 26, further comprising an insulating film interposed between the semiconductor substrate and the semiconductor region, wherein:

the trench penetrates the semiconductor region and the insulating film to reach the semiconductor substrate.

29. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type, having a main surface and a back surface;

a power MOSFET formed in the semiconductor substrate; and

a peripheral device formed in the semiconductor substrate,

wherein the power MOSFET comprises:

a drift region of the first conductivity type extending in the semiconductor substrate from the main surface in a perpendicular direction with respect to the main surface;

a base region of a second conductivity type extending in the drift region from the main surface in the

perpendicular direction;

a source region of the first conductivity type extending in the base region from the main surface in the perpendicular direction;

a trench extending from the main surface in the perpendicular direction, and penetrating the base region from the source region to the drift region;

a gate insulating film provided on an inner wall of the trench; and

a gate electrode provided on a surface of the gate insulating film and filling an inside of the trench, and

wherein the peripheral device is a first conductivity type channel MOSFET, and comprises:

a well layer of the first conductivity type extending in the semiconductor substrate from the main surface in the perpendicular direction;

a base region of the second conductivity type extending in the well layer from the main surface in the perpendicular direction;

a semiconductor region of the first conductivity type extending in the base region from the main surface in the perpendicular direction;

a trench extending from the main surface in the perpendicular direction and dividing the semiconductor region into a source region and a drain region;

a gate insulating film provided on an inner wall

of the trench; and

a gate electrode provided on a surface of the gate insulating film and filling an inside of the trench.

30. The semiconductor device according to claim 29, wherein the semiconductor device is manufactured by:

forming the drift region of the power MOSFET and the well layer of the peripheral device simultaneously;

forming the base region of the power MOSFET and the base region of the peripheral device simultaneously;

forming the source region of the power MOSFET and the semiconductor region of the peripheral device simultaneously;

forming the trench of the power MOSFET and the trench of the peripheral device simultaneously;

forming the gate insulating film of the power MOSFET and the gate insulating film of the peripheral device simultaneously; and

forming the gate electrode of the power MOSFET and the gate electrode of the peripheral device simultaneously.

31. The semiconductor device according to claim 29, further comprising first and second peripheral devices each of which is the first conductivity type channel MOSFET comprising the well layer, the base region, the semiconductor region divided into the source region and the drain region by the trench, the gate insulating film and the

gate electrode, wherein:

the base region of the first peripheral device and the base region of the second peripheral device are electrically separated from each other by an isolation trench extending from the main surface in the perpendicular direction, an insulating film provided on an inner wall of the isolation trench, and a poly silicon layer provided on a surface of the isolation insulating film and filling the isolation trench.

32. The semiconductor device according to claim 31, wherein the semiconductor device is manufactured by;

forming the trench of each of the first and second peripheral devices and the isolation trench simultaneously;

forming the gate insulating film of each of the first and second peripheral devices and the isolation insulating film simultaneously; and

forming the gate electrode of each of the first and second peripheral devices and the poly silicon layer simultaneously.

33. The semiconductor device according to claim 29, wherein the peripheral device further includes a second conductivity type channel MOSFET comprising:

a trench extending in the well layer from the main surface in the perpendicular direction;

a gate insulating film provided on an inner wall

of the trench;

a gate electrode provided on a surface of the gate insulating film and filling the trench;

a source region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at a side of the trench; and

a drain region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at the side of the trench, the drain being separated from the source region.

34. The semiconductor device according to claim 33, wherein the source region and the drain region of the second conductivity type channel MOSFET are provided at both sides of the trench thereof.

35. The semiconductor device according to claim 33, wherein, in the second conductivity type channel MOSFET, the source region surrounds a first end portion of the trench, and the drain region surrounds a second end portion of the trench opposite to the first end portion in a direction parallel to the main surface of the semiconductor substrate.

36. The semiconductor device according to claim 29, the power MOSFET further includes a high-concentration contact region of the second conductivity type extending in the base region from the main surface in the perpendicular

direction and having an impurity concentration higher than that of the base region.

37. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type, having a main surface and a back surface;

a power MOSFET formed in the semiconductor substrate; and

a peripheral device formed in the semiconductor substrate,

wherein the power MOSFET comprises:

a drift region of the first conductivity type extending in the semiconductor substrate from the main surface in a perpendicular direction with respect to the main surface;

a base region of a second conductivity type extending in the drift region from the main surface in the perpendicular direction;

a source region of the first conductivity type extending in the base region from the main surface in the perpendicular direction;

a trench extending from the main surface in the perpendicular direction, and penetrating the base region from the source region to the drift region;

a gate insulating film provided on an inner wall of the trench; and

a gate electrode provided on a surface of the

gate insulating film and filling an inside of the trench, and

wherein the peripheral device is a second conductivity type channel MOSFET, and comprises:

a well layer of the first conductivity type extending in the semiconductor substrate from the main surface in the perpendicular direction, and having an impurity concentration lower than that of the semiconductor substrate;

a trench extending in the well layer from the main surface in the perpendicular direction;

a gate insulating film provided on an inner wall of the trench;

a gate electrode provided on a surface of the gate insulating film and filling the trench;

a source region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at a side of the trench; and

a drain region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at the side of the trench, the drain region being separated from the source region.

38. The semiconductor device according to claim 37, wherein the power MOSFET further comprises a high-concentration contact region of the second conductivity type extending in the base region from the main surface in the

perpendicular direction and having an impurity concentration higher than that of the base region.

39. The semiconductor device according to claim 38, manufactured by:

forming the drift region of the power MOSFET and the well layer of the peripheral device simultaneously;

forming the high-concentration contact region of the power MOSFET and the source region and the drain region of the peripheral device simultaneously;

forming the trench of the power MOSFET and the trench of the peripheral device simultaneously;

forming the gate insulating film of the power MOSFET and the gate insulating film of the peripheral device simultaneously; and

forming the gate electrode of the power MOSFET and the gate electrode of the peripheral device simultaneously.

40. The semiconductor device according to claim 37, wherein the source region and the drain region of the second conductivity type channel MOSFET are provided at both sides of the trench thereof.

41. The semiconductor device according to claim 37, wherein, in the second conductivity type channel MOSFET, the source region surrounds a first end portion of the trench, and the drain region surrounds a second end portion of the

trench opposite to the first end portion in a direction parallel to the main surface of the semiconductor substrate.

42. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type and having a main surface with a first area where a power MOSFET is provided and a second area where a peripheral device is provided;

first and second semiconductor regions of the first conductivity type, respectively provided in the semiconductor substrate at the first area and the second area and having impurity concentrations approximately equal to each other and lower than that of the semiconductor substrate;

first and second trenches respectively extending in the first and second semiconductor regions and having depths approximately equal to each other;

first and second insulating films respectively provided on inner walls of the first and second trenches; and

first and second conductive members respectively filling the first and second trenches with the first and second insulating films interposed therebetween, wherein:

the power MOSFET is composed of the first semiconductor region as a drift region, a base region of a second conductivity type extending in the drift region, a source region of the first conductivity type extending in

the base region, the first insulating film as a gate insulating film, and the first conductive member as a gate electrode that extends to face the drift region, the base region, and the source region via the gate insulating layer; and

the peripheral device is a MOSFET composed of the second semiconductor region as a well layer, the second insulating film as a gate insulating film, the second conductive member as a gate electrode, source and drain regions provided in the well layer separately from each other, the source and drain regions facing the gate electrode with the gate electrode interposed therebetween.

43. The semiconductor device according to claim 42, wherein:

the peripheral device is a first conductivity type channel MOSFET, and further includes a base region of the second conductivity type having a depth approximately equal to that of the base region of the power MOSFET; and

the source and drain regions of the peripheral device are of the first conductivity type and have a depth approximately equal to that of the source region of the power MOSFET.

43. The semiconductor device according to claim 42, wherein:

the peripheral device is a second conductivity type

channel MOSFET; and

the source and drain regions of the peripheral device are of the second conductivity type.